WHAT IS CLAIMED IS:

1. A process of acquiring, transmitting and reconstructing data signals, said process comprising:

monitoring a timing reference signal and a sample interval signal produced by a timing reference;

receiving an input data signal on an input/output module;

sampling the input data signal using one of an external sample clock and an internal sample clock;

measuring an input rate, based on a number of samples received during a sample interval, a duration count, based on a number of cycles of the timing reference signal between a first sample and a last sample received during the sample interval, and a delay count, based on a number of cycles of the timing reference signal received between a start of the sample interval and a first sample clock cycle of the one of the external sample clock and the internal sample clock;

creating data packets, based on sampled input data and the measured input rate, and the measured delay count for each sample interval;

transmitting the data packets;

receiving the data packets; and

reconstructing the input data signal based on the data packets.

2. A process as recited in claim 1, wherein said step of transmitting the data packets comprises transmitting the data packets over a network and said step of

receiving the data packets comprises receiving the data packets over the network.

3. A process as recited in claim 1, wherein said step of transmitting the data packets comprises storing the data packets on a storage medium and said step of receiving the data packets comprises retrieving the data packets from the storage medium.

4. A process as recited in claim 1, further comprising transferring the data packets to a central processing unit and said step of transmitting the data packets is performed by the central processing unit.

5. A process as recited in claim 1, wherein said step of monitoring a timing reference signal produced by a timing reference comprises monitoring the timing reference signal and an end of interval signal produced by the timing reference.

6. A process of processing data signals, said process comprising:

monitoring a timing reference signal produced by a timing reference;

receiving input data signals on input/output modules;

sampling the input data signals using one of an external sample clock and an internal sample clock;

measuring an input rate, based on a number of samples received during a sample interval, a duration count, based on a number of cycles of the timing reference signal

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between a first sample and a last sample received during the sample interval, and a delay count, based on a number of cycles of the timing reference signal received between a start of the sample interval and a first sample clock cycle of the one of the external sample clock and the internal sample clock;

creating data packets, based on sampled input data and the measured input rate, and the measured delay count for each sample interval.

7. A process as recited in claim 6, further comprising transmitting the data packets over a network.

8. A process as recited in claim 6, further comprising storing the data packets on a storage medium.

9. A process as recited in claim 6, further comprising transferring the data packets to a central processing unit and said step of transmitting the data packets is performed by the central processing unit.

10. A process as recited in claim 6, wherein said step of monitoring a timing reference signal produced by a timing reference comprises monitoring the timing reference signal and an end of interval signal produced by the timing reference.

11. A process of reconstructing data signals, said process comprising:

receiving data packets;

retrieving an input rate, based on a number of samples acquired during a sample interval in an original data signal, a duration count, based on a number of cycles of a timing reference signal received between a first sample clock and a last sample clock in the sample interval, and a delay count, based on a number of cycles of the timing reference signal received between a start of the interval and a first sample clock cycle of a sample clock in the original data signal;

determining a measured data rate and a phase offset for the original data signal, based on sampled input data and the input rate, the duration count and the delay count for each interval; and

reconstructing the original data signal based on input data contained in the data packets and the determined measured data rate and phase offset.

12. A process as recited in claim 11, wherein said step receiving data packets comprises receiving data packets over a network.

13. A process as recited in claim 11, wherein said step receiving data packets comprises retrieving data packets from a storage medium.

14. A process as recited in claim 11, wherein said step of determining a measured data rate and a phase offset for the original data signal comprises providing a direct digital synthesizer with rate control data, receiving a reconstructed clock signal

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from the direct digital synthesizer and determining the measured data rate and the phase

5   offset for the original data signal based on sampled input data and the input rate, the

duration count, the delay count for each interval and the reconstructed clock signal.

15. A system for acquiring, distributing and reconstructing data signals, said

system comprising:

input/output modules, sending and receiving data signals and sample clock

signals;

5   a timing reference, providing a reference clock signal and an end of interval

signal to each of the input/output modules;

a central processing unit, sending and receiving data packets to and from the

input/output modules; and

a data packet interface in communication with the central processing unit, for

10   sending and receiving data packet to and from at least one of a network and a data

storage medium;

wherein input/output modules are configured to create data packets based on

sampled input data and an input rate, a duration count and a delay count for each

interval of the data signals and are configured to reconstruct an original data signal

15   based on input data contained in the data packets and a measured data rate and a

determined phase offset.

16. A system as recited in claim 15, wherein each input/output module of said

input/output modules comprises a signal acquisition unit and a signal reconstruction unit, wherein the signal acquisition unit receives data signals, the reference clock signal and the end of interval signal and outputs data packets, and wherein the signal

5 reconstruction unit receives data packets, the reference clock signal and the end of interval signal and outputs the original data signal.

17. A system as recited in claim 16, wherein each input/output module of said input/output modules further comprises a direct digital synthesizer, wherein the direct digital synthesizer receives a rate control signal from the signal reconstruction unit and provides a reconstructed clock signal to the signal reconstruction unit.

18. A system as recited in claim 15, wherein said step receiving data packets comprises retrieving data packets from a storage medium.